

WHAT IS CLAIMED IS:

1. A ferroelectric memory comprising:

a memory cell including a ferroelectric capacitor  
5 having a ferroelectric film capable of taking different  
electric capacitances  $C_{f0}$  and  $C_{f1}$  in an initial state and  
first and second electrodes formed to hold said  
ferroelectric film therebetween;

a circuit applying a read voltage  $V_R$  to said first  
10 electrode; and

a detector capable of detecting the difference  
between the electric capacitances  $C_{f0}$  and  $C_{f1}$  of said  
ferroelectric film when the potential difference of said  
second electrode corresponding to the difference between  
15 the electric capacitances  $C_{f0}$  and  $C_{f1}$  of said ferroelectric  
film is in excess of a detection limit voltage  $V_S$ , wherein

the electric capacitance  $C_2$  of said second electrode  
is set to satisfy the following expression:

$$C_{f0} < C_2 \leq 1/2 \times \{(C_{f1} - C_{f0})V_R/V_S - (C_{f1} + C_{f0})\}$$

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2. The ferroelectric memory according to claim 1,  
wherein

the electric capacitance  $C_2$  of said second electrode  
is substantially expressed as follows:

25  $C_2 = (C_{f1} \times C_{f0})^{1/2}$

3. The ferroelectric memory according to claim 1,  
wherein

a voltage applied to said ferroelectric film is less  
5 than a voltage causing polarization inversion of said  
ferroelectric film when holding data in a polarization  
direction opposite to the direction of application of said  
read voltage in data reading.

10 4. The ferroelectric memory according to claim 3,  
wherein

said voltage applied to said ferroelectric film is  
greater than said voltage causing polarization inversion  
of said ferroelectric film when holding data in a  
15 polarization direction identical to the direction of  
application of said read voltage in data reading.

5. The ferroelectric memory according to claim 1,  
wherein

20 said memory cell includes a memory cell having said  
second electrode connected with a gate electrode of a  
transistor.

6. The ferroelectric memory according to claim 5,  
25 wherein

said detector includes a current sense amplifier.

7. The ferroelectric memory according to claim 5,  
wherein

5       said first electrode is connected to a word line.

8. The ferroelectric memory according to claim 3,  
wherein

10       said memory cell includes a memory cell constituted  
of a ferroelectric capacitor consisting of said first  
electrode and said second electrode formed to extend in  
directions intersecting with each other and said  
ferroelectric film arranged between said first electrode  
and said second electrode.

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9. The ferroelectric memory according to claim 8,  
wherein

said detector includes a voltage sense amplifier.

20       10. The ferroelectric memory according to claim 8,  
wherein

said first electrode is a word line, and  
said second electrode is a bit line.

25       11. The ferroelectric memory according to claim 3,

wherein

said memory cell includes a memory cell having said second electrode connected to either a source region or a drain region of a transistor.

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12. The ferroelectric memory according to claim 11,  
wherein

said detector includes a voltage sense amplifier.

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13. The ferroelectric memory according to claim 11,  
wherein

said first electrode is connected to a plate line.

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14. The ferroelectric memory according to claim 1,  
further comprising a row decoder selecting said first  
electrode corresponding to a row address,

said row decoder including said circuit applying said  
read voltage  $V_R$  to said first electrode.

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15. The ferroelectric memory according to claim 1,  
wherein

said initial state is an initial state applying no  
voltage.

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16. A ferroelectric memory comprising:

a memory cell including a ferroelectric capacitor having a ferroelectric film capable of taking different electric capacitances  $C_{f0}$  and  $C_{f1}$  in an initial state and first and second electrodes formed to hold said

5 ferroelectric film therebetween;

means applying a read voltage  $V_R$  to said first electrode; and

detection means capable of detecting the difference between the electric capacitances  $C_{f0}$  and  $C_{f1}$  of said  
10 ferroelectric film when the potential difference of said second electrode corresponding to the difference between the electric capacitances  $C_{f0}$  and  $C_{f1}$  of said ferroelectric film is in excess of a detection limit voltage  $V_S$ , wherein

the electric capacitance  $C_2$  of said second electrode  
15 is set to satisfy the following expression:

$$C_{f0} < C_2 \leq 1/2 \times \{(C_{f1} - C_{f0})V_R/V_S - (C_{f1} + C_{f0})\}$$

17. The ferroelectric memory according to claim 16,  
wherein

20 the electric capacitance  $C_2$  of said second electrode is substantially expressed as follows:

$$C_2 = (C_{f1} \times C_{f0})^{1/2}$$

18. The ferroelectric memory according to claim 16,  
25 wherein

a voltage applied to said ferroelectric film is less than a voltage causing polarization inversion of said ferroelectric film when holding data in a polarization direction opposite to the direction of application of said  
5 read voltage in data reading.

19. The ferroelectric memory according to claim 16, wherein

said memory cell includes a memory cell having said  
10 second electrode connected with a gate electrode of a transistor.

20. The ferroelectric memory according to claim 18, wherein

15 said memory cell includes a memory cell constituted of a ferroelectric capacitor consisting of said first electrode and said second electrode formed to extend in directions intersecting with each other and said ferroelectric film arranged between said first electrode  
20 and said second electrode.

21. The ferroelectric memory according to claim 18, wherein

said memory cell includes a memory cell having said  
25 second electrode connected to either a source region or a

drain region of a transistor.

22. The ferroelectric memory according to claim 16,  
wherein

5       said initial state is an initial state applying no  
voltage.